

IN THE CLAIMS

1. (Original) A method of forming a germanium-on-insulator (GOI) substrate comprising:
 - forming an epitaxial germanium layer on top of a first substrate;
 - forming a first dielectric film on top of the epitaxial germanium layer;
 - providing a second substrate;
 - bonding the first substrate to the second substrate by bonding the first dielectric film to the second substrate, the bonding resulted in a bonded wafer pair;
 - and
 - removing the first substrate after the bonding to expose epitaxial germanium layer to form the GOI substrate.
2. (Withdrawn) A method as in claim 1 further comprises forming a second dielectric film on top of the second substrate wherein the bonding of the first substrate to the second substrate further comprises bonding the first dielectric film to the second dielectric film.
3. (Original) A method as in claim 1 wherein the removing of the first substrate after the bonding includes one of a grind back process, an etching process, and an ion exfoliation process.

4. (Original) A method as in claim 1 further comprising:

polishing the surface of the first dielectric film prior to the bonding.
5. (Original) A method as in claim 1 further comprises causing an ion implantation to the first substrate through the first dielectric film to define a cleaving plane.
6. (Withdrawn) A method as in claim 5 further comprises forming a second dielectric film on top of the second substrate wherein the bonding of the first substrate to the second substrate further comprises bonding the first dielectric film to the second dielectric film.
7. (Currently Amended) A method as in claim ~~[[7]]~~ 1 wherein the removing of the first substrate after the bonding includes cleaving off the first substrate.
8. (Original) A method as in claim 5 further comprising:

polishing the surface of the first dielectric film after the ion implantation, the polishing performs at least one of providing a smooth surface for the first dielectric film, repairing surface damages on the first dielectric film, and providing a clean surface for bonding.

9. (Original) A method as in claim 1 wherein each of the first substrate and the second substrate semiconductor wafer is selected from a group consisting of a silicon (Si) substrate, a monocrystalline Si substrate, a polycrystalline Si substrate, a Si-containing substrate, a Si substrate having an oxide layer, a silicon-on-insulator (SOI) substrate, a gallium arsenide substrate, and Ge-containing substrate.
10. (Original) A method as in claim 1 further comprising causing a surface activation to the top surface of the first dielectric film and at least one surface of the second substrate to facilitate the bonding.
11. (Original) A method as in claim 1 further comprises annealing the bonded wafer pair at a predetermined annealing temperature, wherein the annealing temperature is achieved with a temperature ramp rate of approximately 1°C/minute.
12. (Original) A method of bonding a germanium layer having a rough surface to a substrate comprising:
- forming an epitaxial germanium layer on top of a first substrate, the epitaxial germanium layer having a rough surface, the rough surface has a roughness value approximately greater than 2nm RMS;
 - forming a first dielectric film on top of the rough surface;

bonding the first dielectric film to a second substrate, the bonding resulted in a bonded wafer pair wherein the first dielectric film is located between the epitaxial germanium layer and the second substrate; and

removing the first substrate after the bonding to expose epitaxial germanium layer.

13. (Withdrawn) A method as in claim 12 further comprises forming a second dielectric film on top of the second substrate wherein the bonding of the first dielectric film to the second substrate includes bonding the first dielectric film to the second dielectric film.
14. (Original) A method as in claim 12 wherein the removing of the first substrate after the bonding includes one of a grind back process, an etching process, and an ion exfoliation process.
15. (Original) A method as in claim 12 further comprising:

polishing the surface of the first dielectric film prior to the bonding.
16. (Original) A method as in claim 12 further comprises causing an ion implantation to the first substrate through the first dielectric film to define a cleaving plane.

17. (Original) A method as in claim 16 wherein the removing of the first substrate after the bonding includes cleaving off the first substrate.
18. (Original) A method as in claim 17 further comprising:
polishing the surface of the first dielectric film after the ion implantation, the polishing performs at least one of providing a smooth surface for the first dielectric film, repairing surface damages on the first dielectric film, and providing a clean surface for bonding.
19. (Original) A method as in claim 12 wherein each of the first substrate and the second substrate semiconductor wafer is selected from a group consisting of a silicon (Si) substrate, a monocrystalline Si substrate, a polycrystalline Si substrate, a Si-containing substrate, a Si substrate having an oxide layer, a silicon-on-insulator (SOI) substrate, a gallium arsenide substrate, and Ge-containing substrate.
20. (Original) A method as in claim 12 further comprising causing a surface activation to the top surface of the first dielectric film and at least one surface of the second substrate to facilitate the bonding.
21. (Original) A method as in claim 12 further comprises annealing the bonded wafer pair at a predetermined annealing temperature, wherein the annealing temperature is achieved with a temperature ramp rate of approximately 1°C/minute.

22. (Original) A method of fabricating a semiconductor device comprising:
- forming an epitaxial germanium layer on top of a first substrate;
 - forming a first dielectric film on top of the epitaxial germanium layer;
 - providing a second substrate;
 - bonding the first substrate to the second substrate by bonding the first dielectric film to the second substrate, the bonding resulted in a bonded wafer pair;
 - removing the first substrate after the bonding to expose epitaxial germanium layer to form a GOI substrate; and
 - forming an electronic device on the GOI substrate.
23. (Original) A method as in claim 22 wherein the electronic device includes one of a transistor and a detector.
24. (Original) A method as in claim 23 wherein the transistor includes a gate dielectric, a gate electrode, spacers and source/drain regions.
25. (Original) A method as in claim 23 wherein the detector includes a waveguide encapsulated by an oxide layer and at least one electrode.
26. (Withdrawn) A method as in claim 22 further comprises forming a second dielectric film on top of the second substrate wherein the bonding of the first substrate to the

second substrate further comprises bonding the first dielectric film to the second dielectric film.

27. (Original) A method as in claim 22 wherein the removing of the first substrate after the bonding includes one of a grind back process, an etching process, and an ion exfoliation process.

28. (Original) A method as in claim 22 further comprising:

polishing the surface of the first dielectric film prior to the bonding.

29. (Original) A method as in claim 22 further comprises causing an ion implantation to the first substrate through the first dielectric film to define a cleaving plane.

30. (Original) A method as in claim 22 wherein the removing of the first substrate after the bonding includes cleaving off the first substrate.

31. (Withdrawn) A semiconductor assembly comprising:

an epitaxial germanium layer formed on top of a first substrate, the epitaxial germanium layer having a rough surface;

a first dielectric film is formed on top of the epitaxial germanium layer over the rough surface;

a second substrate bonding to the first substrate with the first dielectric film bonding to the second substrate, the bonding resulted in a bonded wafer pair; and wherein the first substrate is removeable after the bonding to expose epitaxial germanium layer to form a GOI substrate.

32. (Withdrawn) A semiconductor assembly as in claim 31 wherein the rough surface has a roughness value approximately greater than 2nm RMS.